

**IN THE SPECIFICATION:**

The "Brief Description of the Drawings" section at page 5, line 21, through page 6, line 9, was replaced by a rewritten section in an Amendment filed on March 24, 2009. **Please replace** this rewritten section with the following revised rewritten section:

**Brief Description of the Drawings**

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a view showing problems on dry etching of gate electrodes employed in a prior art;

Fig. 2 is a view illustrating dry-etched shapes of the gate electrodes employed in the prior art; and

Fig. 3 is a dry etching process sectional view for describing an embodiment of the present ~~invention~~, and invention.

~~Figure 4 is a top view of the arrangement shown in Figure 3.~~

The Amendment filed on March 24, 2008 also replaced the paragraph at page 6, lines 11-26, with a rewritten paragraph. **Please replace** this rewritten paragraph with the following revised rewritten paragraph:

A first embodiment of the present invention will be explained. Although not shown in the drawing, a gate insulating film is formed on a silicon substrate 1 and thereafter a polysilicon layer 2 constituted as gate electrodes is deposited thereon. Next, a resist 3 is subjected to patterning. ~~Phosphor~~ Phosphorous (P) ions are selectively implanted into a region 4 for forming an N type channel transistor gate (see Fig. 3(a)). Boron (B) ions are selectively implanted into a region 5 for forming a P type channel

transistor gate (see Fig. 3(b)). At this time, no impurity is injected into a dummy gate electrode region 6. Subsequently, patterning is done by a lithography technique and the non-doped polysilicon and doped polysilicon regions 4 and 5 and in the dummy gate electrode region 6 are etched to form gate electrodes ~~7 and 8 and a dummy gate arrangement 9~~ (see Fig. 3(c)).

An Amendment filed on July 12, 2005 added two new paragraphs at the end of page 6 or top of page 7, and these two new paragraphs were subsequently rewritten in an Amendment filed on April 27, 2006. **Please replace** these rewritten paragraphs with the following revised rewritten paragraphs:

In Figs. 3(a)- 3(c), the line break on the right side indicates that region 6 may extend horizontally in the figures farther than is ~~shown~~. shown, such that an area of the region 6 would be greater than an area of the region 4 and/or region 5. Even without taking the break into account, Fig. 3(c) shows that the area occupied by the etched non-doped polysilicon region 6 dummy gate pattern is larger than the total area occupied by the N-type and P-type polysilicon regions ~~gates~~ which have been etched.

Figs. 3(a) -3(c) also show how the regions are contiguous.